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B.Tech –II Sem

Basic Electronics Engineering (EC-201)

FET AND MOSFET

Page

Field effect Transistor (FET)

- The operation of the device depends on electric field intensity produced in the channel.
- Voltage controlled device.
- High Ω /P resistance device ($\geq 1M\Omega$)
- Lower dissipation is very small.
- Unipolar device
- Majority Carrier device.
- No minority carriers.
- Less noisy device than BJT, due to absence of minority carriers.
- No leakage current & therefore temperature effect on the device is very less & therefore excellent thermal stability.
- Fabricated only with Si.
- When compare to BJT, FET is small in size & easier to fabricate.

Disadvantage :-

- Smaller gain
- Smaller gain bandwidth product.

Region of FET

Source :- It is the source of majority carrier.

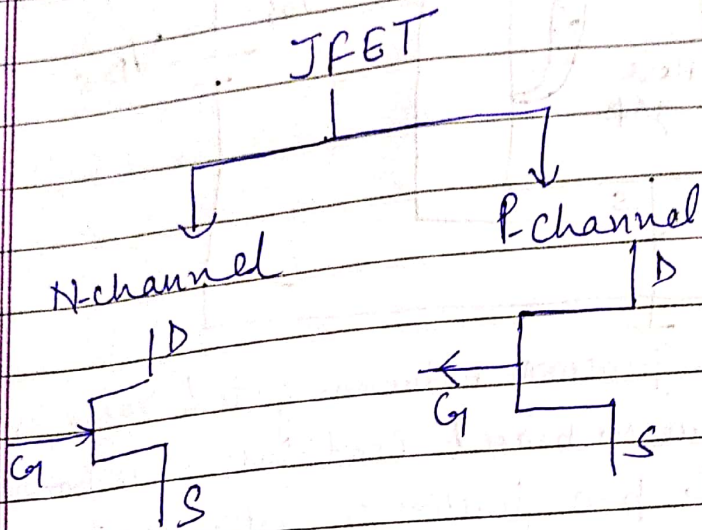
i.e. it is the terminal by which majority carrier will be entering

Drain :- It drains off majority carrier ^{into device}. It is the terminal by which majority carrier will be leaving the device.

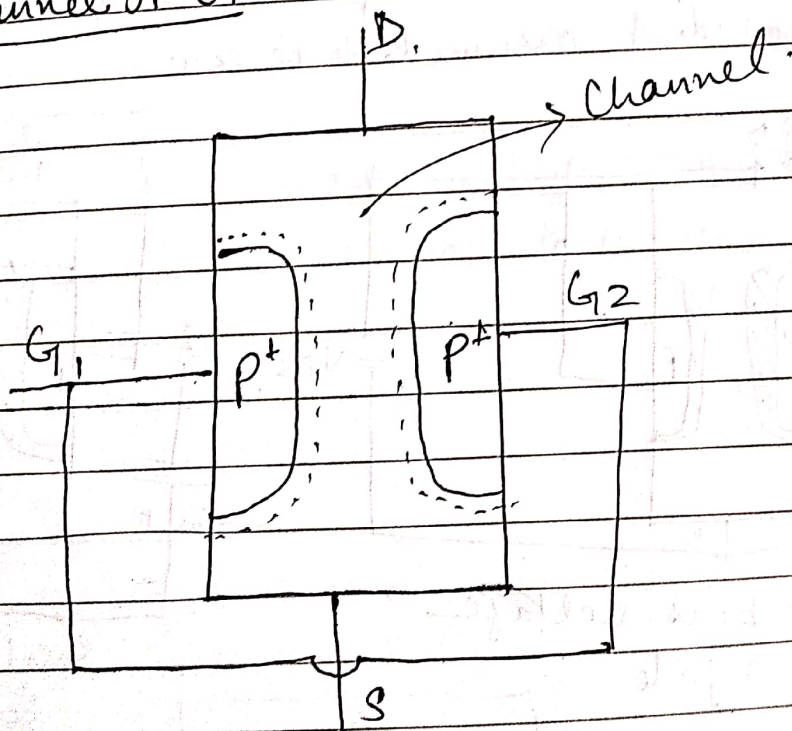
Gate :- It is terminal which control majority

Carriers moving from source to drain.

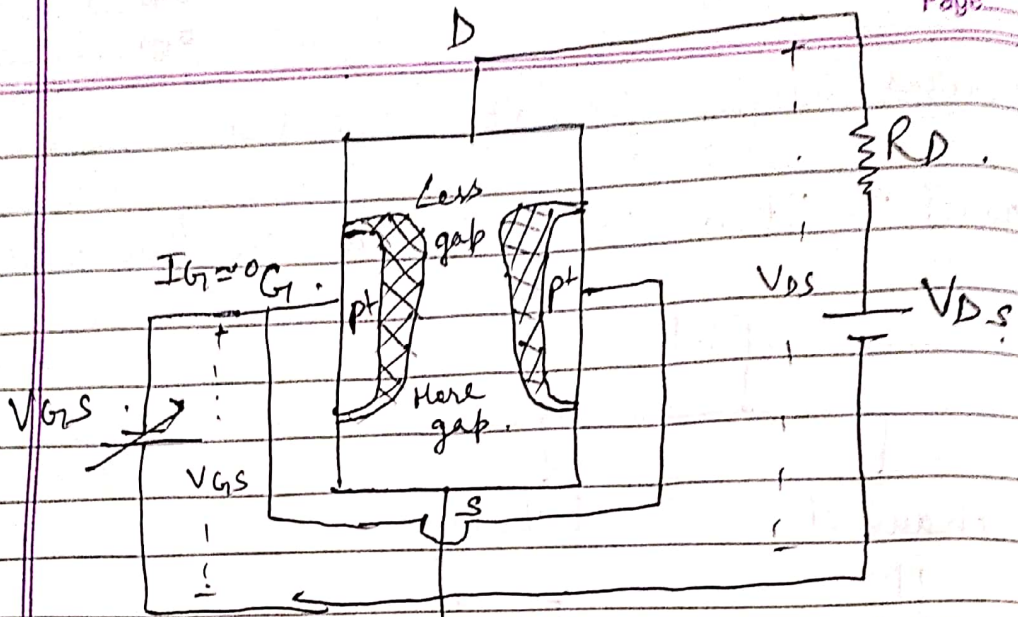
Channel :- It is the region b/w the two gates.



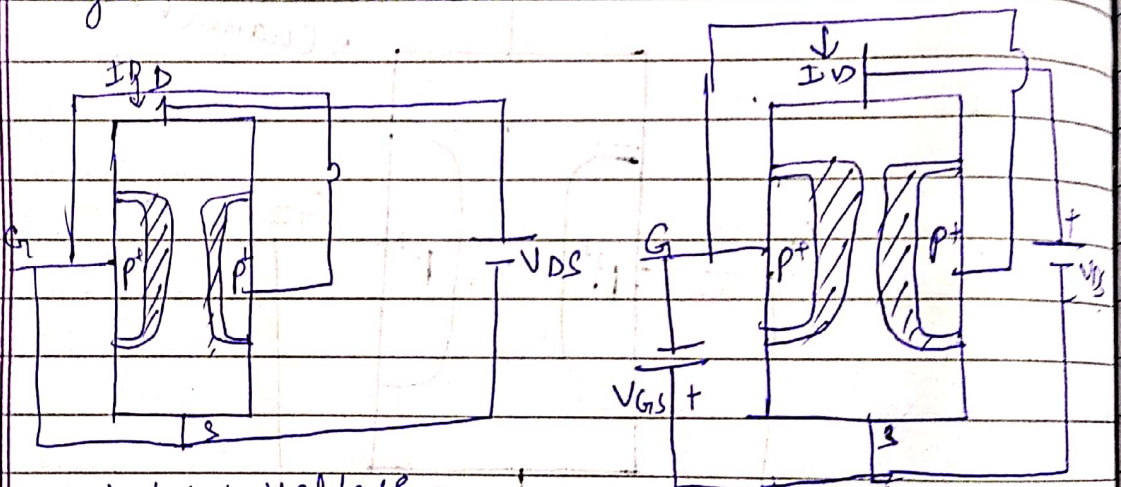
N-channel JFET



→ When JFET is open circuited, channel cross sectional area is maximum & therefore channel current density is minimum.

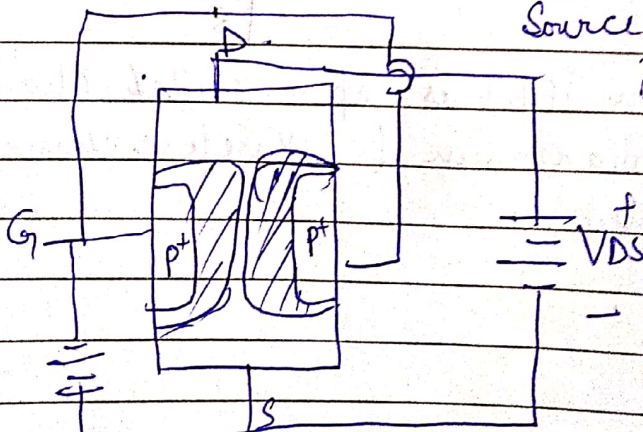


In JFET, the p-n junction between gate & source is always kept in reverse biased conditions. Since current in a reverse biased p-n junction is extremely small, practically zero, the gate current in JFET is often neglected & assumed to be zero.



No bias voltage on gate

Small negative gate source bias fig (a)



Large negative gate source bias fig (b)

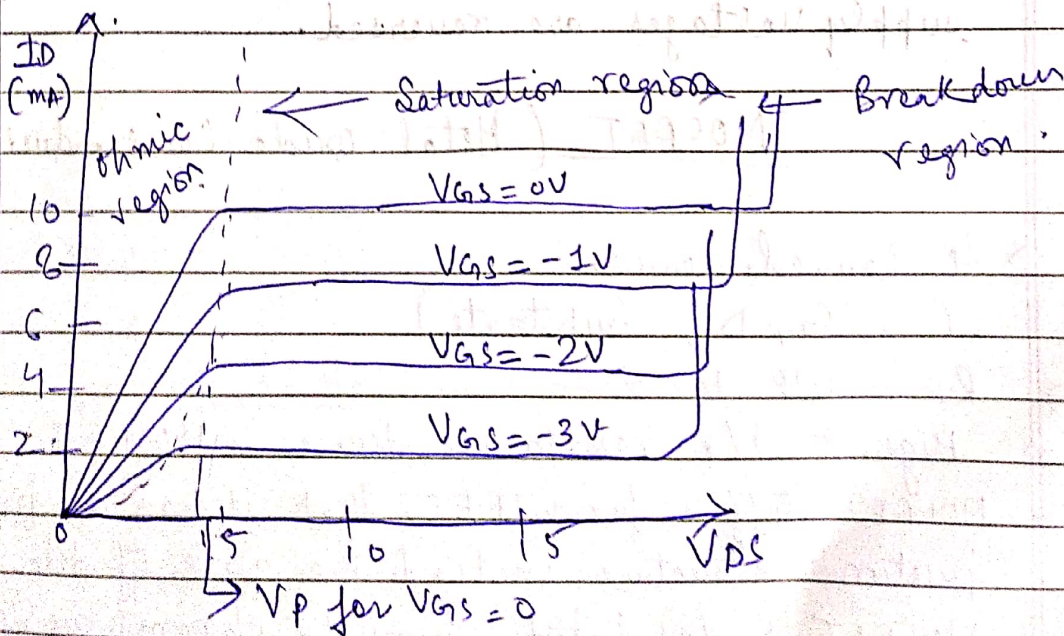
→ when gate to source voltage (V_{GS}) is applied by a dc supply (V_{GS}) and increased above zero as depicted in fig (a) the reverse bias voltage across the gate-source junction is increased. Because of this depletion regions are widened. This reduces the effective width of the channel & hence controls the flow of drain current through the channel.

→ when gate to source voltage is further increased, a stage is reached at which two depletion regions touch each other as shown in fig (b). This condition is called Pinch off.

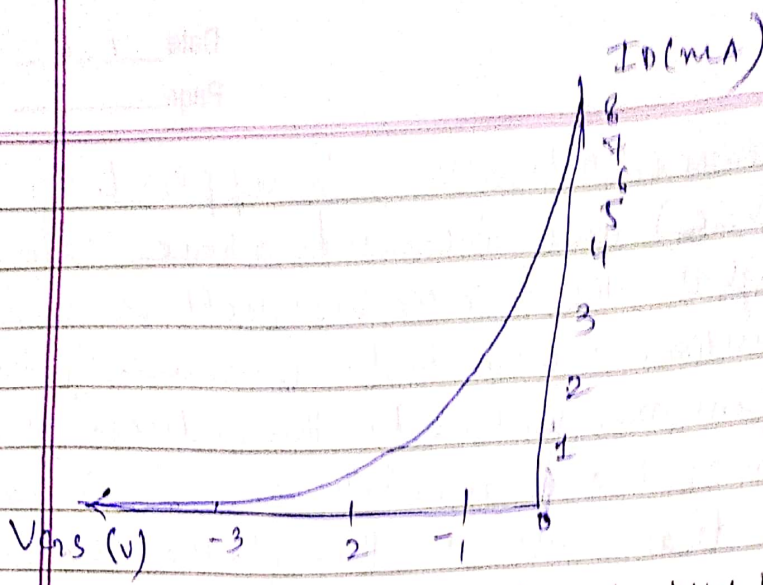
Pinch off Voltage (V_P). It is minimum value of V_{DS} required where I_D enters into Saturation for given value of V_{GS} .

$V_{GS(off)}$ The cut off voltage is the value of V_{GS} at which drain current is zero.

$$V_{GS} = -|V_P|$$



Drain characteristics of n channel JFET



Transfer characteristics of n channel JFET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

The relationship b/w I_D & V_{GS} is non linear
 this relationship is defined by Shockley's equation.

Note:- The operation of p-channel JFET is exactly similar to n-channel JFET except that the current carriers are holes & polarity of supply voltages are reversed.

MOSFET (Metal oxide Semiconductor FET)

- 4 channel devices
 (S, G, D, Substrate)
- $R_i = 10^{10}$ to $10^{15} \Omega$
- Highest g/p resistance device is MOSFET
- MOSFET differs from JFET in that it has no pn junction structure. Instead the gate of the MOSFET is insulated from the channel by SiO_2 layer.

MOSFET

Depletion MOSFET

→ there is a pre-existing channel.

→ Suitable to operate in the depletion mode & enhancement mode.

Enhancement MOSFET

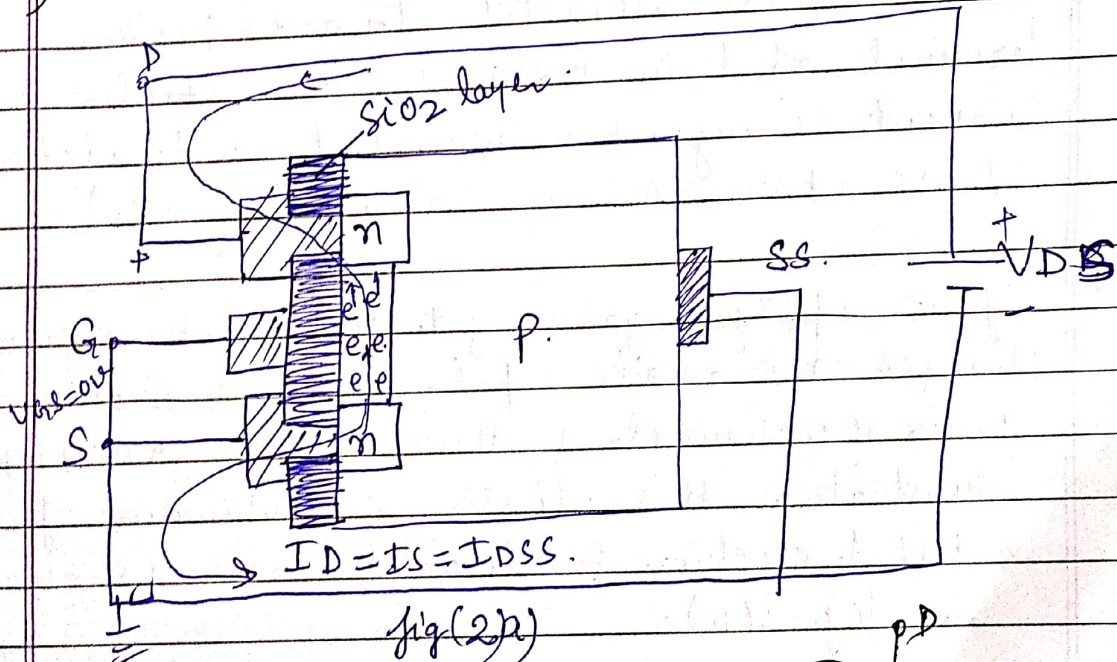
→ no pre existing channel

→ Suitable to operate in the enhance mode only.

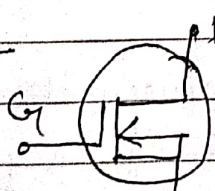
→ Input resistance of MOSFET > Input resistance of JFET
 → Lower dissipation is less < Lower dissipation in JFET.

Depletion MOSFET (D-MOSFET)

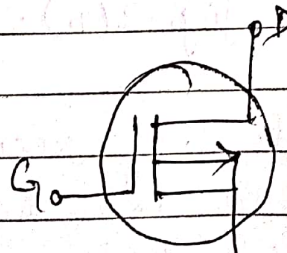
n-channel Depletion MOSFET.



Symbol



n channel depletion type MOSFET



P-channel depletion type MOSFET

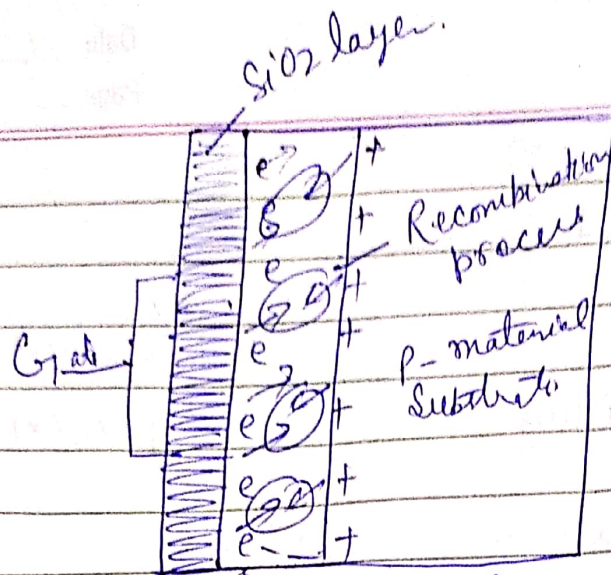


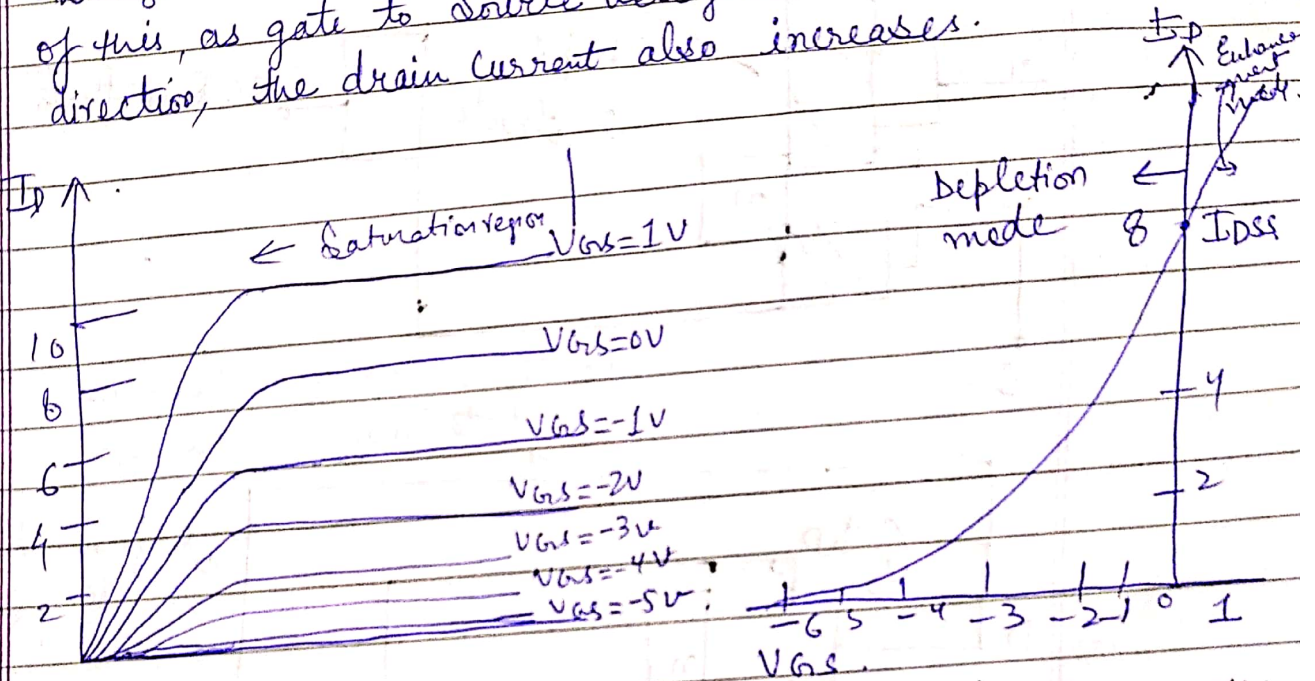
fig 2(b)

(Reduction in free electrons in the n channel due to negative potential at the gate terminal)

- On the application of drain to Source Voltage, V_{DS} & keeping gate to Source Voltage to zero by directly connecting gate terminal to source terminal, free electrons from the n channel are attracted towards positive terminal of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0V$ as shown in fig 2(a),
- if we apply negative gate Voltage, the negative charges on the gate repel conduction electrons from the channel & attract holes from p-type substrate. This initiates recombination of repelled electrons & attracted holes as shown in fig 2(b).
- The level of recombination between electrons & holes depends on the magnitude of negative Voltage applied to the gate. This recombination reduces

The number of free electrons in the n-channel for the conduction reducing the drain current.

For positive value of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current & establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in +ve direction, the drain current also increases.

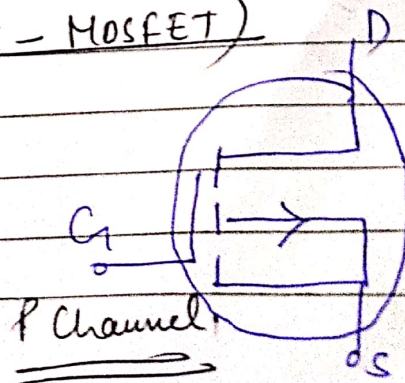
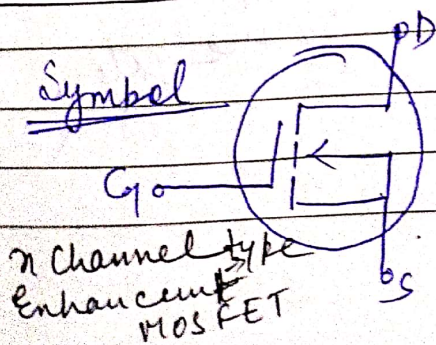


Drain characteristics for an n-channel depletion type MOSFET

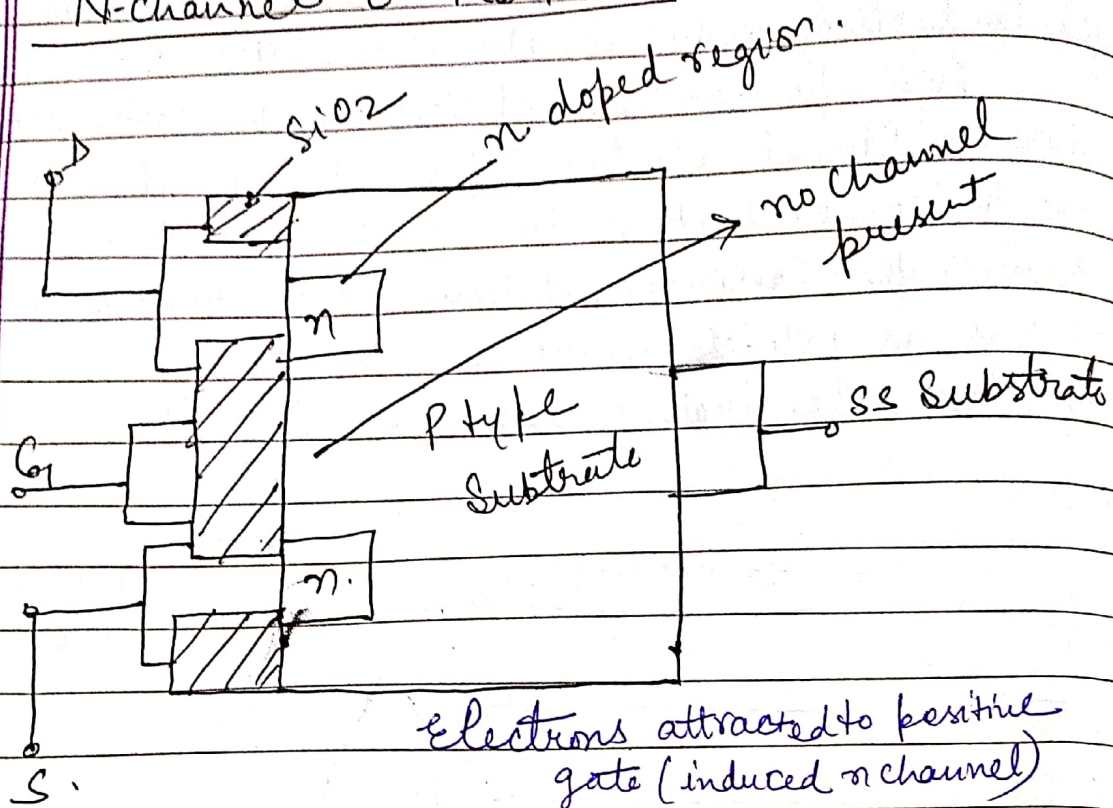
Transfer characteristics for n-channel depletion type MOSFET

Note:- operation of p-channel Depletion MOSFET is exactly similar to n-channel Depletion MOSFET except that of current carrier & polarity of supply voltage.

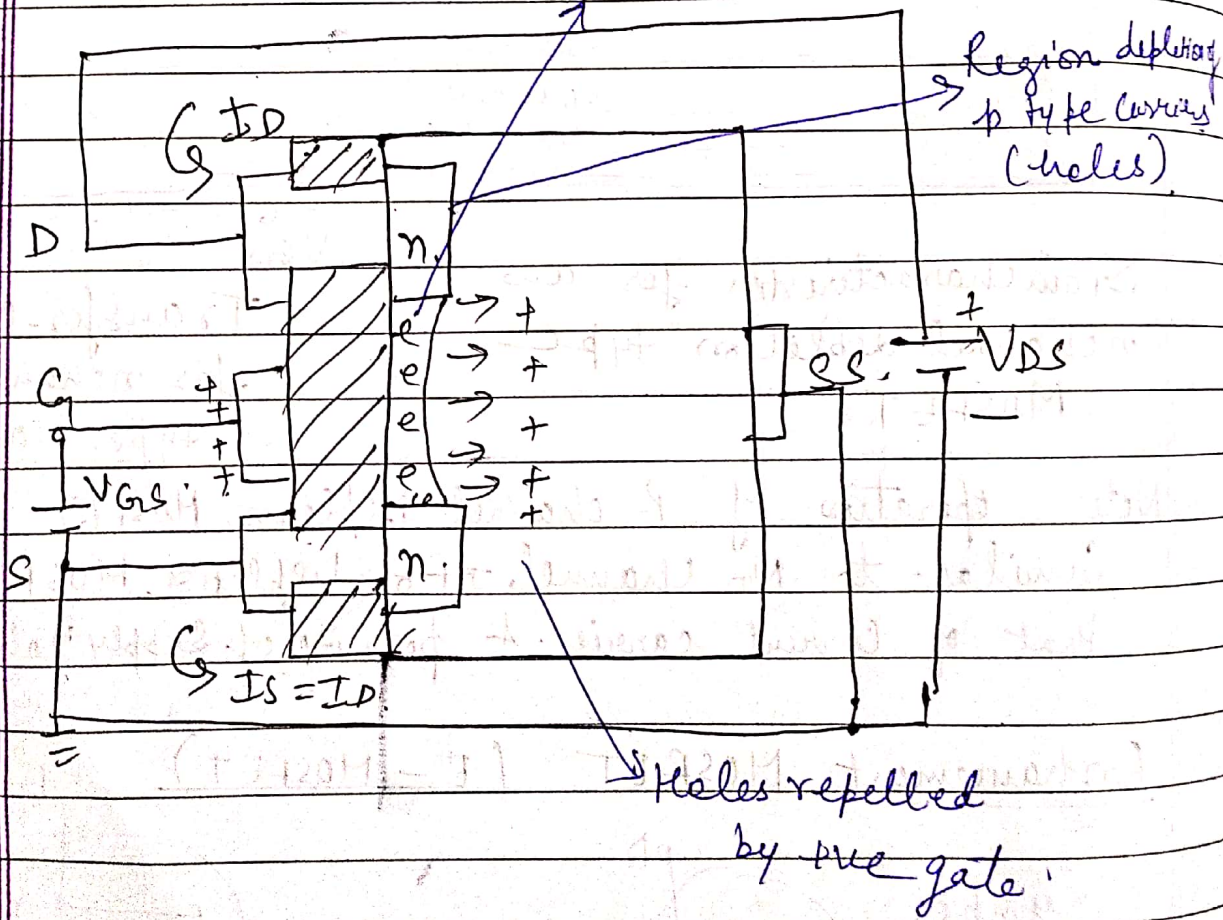
Enhancement MOSFET (E-MOSFET)



N-channel E-MOSFET



Electrons attracted to positive gate (induced n channel)

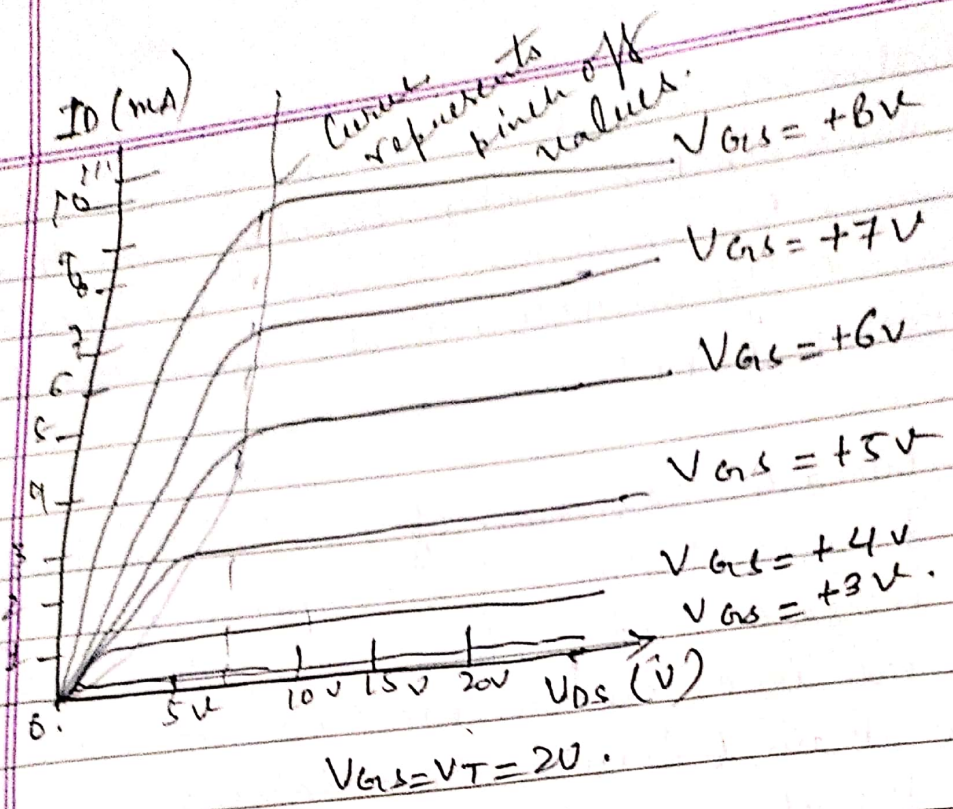


→ On application of drain to source voltage V_{DS} & keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows quite different from the depletion type MOSFET & JFET.

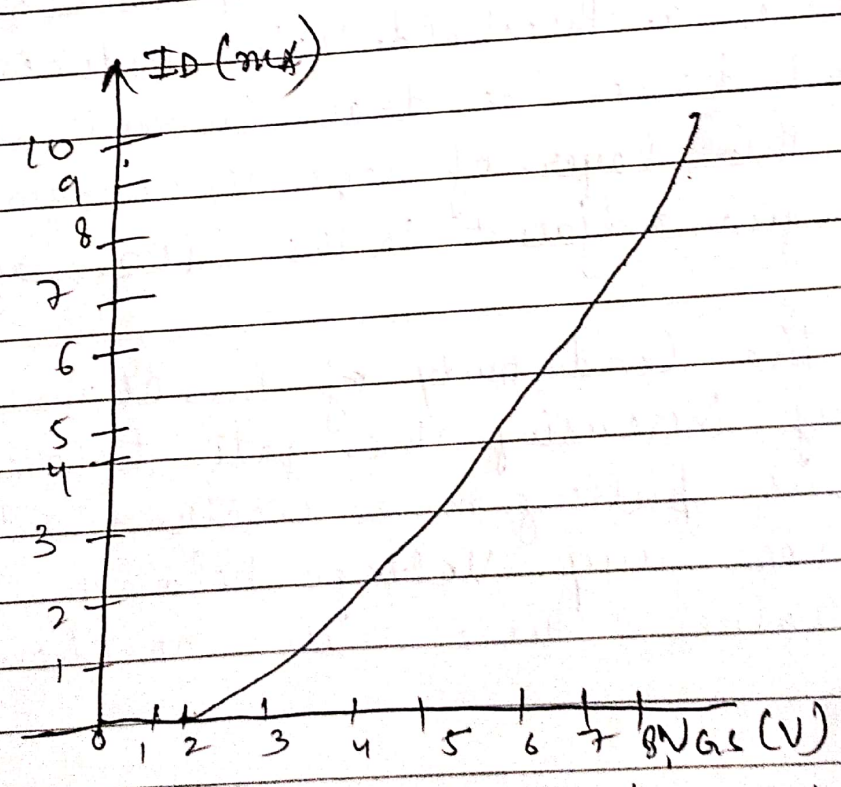
→ If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain & source. This value of V_{GS} is called threshold voltage denoted by V_T .

→ This we can say that in an enhancement type n channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in substrate region adjacent to the SiO_2 layer.

→ The conductivity of the channel is enhanced by increasing the gate to source voltage & thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.



Drain characteristics of an n-channel enhancement type MOSFET.



Transfer characteristics for n channel Enhancement type MOSFET.