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B.Tech –II Sem

Basic Electronics Engineering (EC-201)

Unit-3 OPERATIONAL AMPLIFICADate Page The operational amplifies most commonly referred mas introduced in 1940's. The just op-amp was designed in 1948 using vaccum. Due to the use of nacceum tubes, the early tubes op-amps mere bucky, power consuming and expensive. Due to its use in performing mathematical operations it has been a name operations amplifie. Robert J. Widlas at Fairchild brought popular 741 integrated (IC) opamp between 1364 to 1968. The TC version of opamps BTTS and FETS which are Jabricated along with the other supporting components on a Single Semiconductor chip er majer which is pinhead Size. With the help of Ic op-amp, the Circuit design becomes very simple Of Amp symbol of terminals tesitive supply veltage +VCC Investing input terminal output terminal op-amp Von-inverting fermenal -Vee Negative Supply Wolky

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186° Bluce Page Vo op-amp -VEE inverted output with respect to input a) input applied to investing terminal +VCC op-amp. VEE Non invested output in phase Zero phase shift b) inpet applied to non incerting terminal Saturable property of op-amp <u>A</u>\_\_\_\_\_ the open loop gain of opamp is very high while every of-amp has property that its output Can Swing between two levels decided by supply veltager + Vccl-VEE. There if output tries to rive more than + VCC or less then - VEE thent it gets clipped & get saturated at the levels almost equal to tVCC & - VEE on positive of negative Side respectively. Ideal of-Amp: - The ideal of amp is basically on amplifies which amplifies the difference between

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Date Page. the two input Signals, In its basic form, to opamp is nothing but a differential amplifier. Ideal differential amplifies The differential amplifies amplifies the difference between two input voltage signals. Hence it is also Called difference amplifile Ideal -0 V0. ] Differential amplifie. In an ideal differential amplifier the output Ultage Vo is proportional to the difference between the two input Signals, Hence we can write, Vo x(V,-V2) Ad is the gain with which fferential gain (Ad). > differential amplifier amplifies the difference two input signals Yo = Ad (U,-V Ad = Vo Vd Ad = 20 log 10 Ad in dB. Sommon mode gain (Ac) apply two input voltages which are eque differential amplifier ideally Vo-(V,-V2) But O/P of practical differential amplifier depends on the average common level of two input Such an average level of two input signal to Called common mode Signal.

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Date\_\_\_/ Page\_  $V_{c} = \frac{V_{1} + V_{2}}{2}$   $V_{o} = A_{c} V_{c}$ Total of P of any differential amplifier Vo = AdVd + AcVc Ideal op-amp-\_Va 2+ Aoy Vd. bractical op-amp Ro Vo forVd. TIT Vo Positive Saturations Voltage + Vsat=+Vcq. +VSat -Var. Vd - Va +Vd -Vsat I deally it is straight vertical line Negative Saturation VSat = -VEE a) Ideal Vætage Transfer Curves

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Page CMRR ( Common Mode. Rejection Ratto) The ability of a differential amplifier to reject Common mode Signal is expressed by a ratio Called Common mode Rejection Ration denoted as it is defined as the ratio of the differential Ueltage gain Ad to common mode Voltage CMRR or f. gain Ac CMRR=f= Ad I deally the common made Voltage gain × hence the ideal values of CMRR emplifies Ad is for a practical differential × large & Ac is Small hence the val CMRR is also very large CMRR in dB = 20 log Ad dB Slew Rate > It is defined as the maximum rate of change of output Voltage with time expressed in V/1 Slew rate S Its ideal value is infinite for the span deal op- Amp chara sterities 2) infinite Voltage gain AOL = 15) 2) Infinite Input Impedance (REIN = 20)

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Date Includes Page\_ Zoro output impedance (Ro=0) Zero offset Voltage (Lios=0) Infinite Bandwidth infinite CMRR (f=00) infinite Slew rate (S=w) lover supply rejection ratio (PSRR=0) Ggt is defined as the rates of change in input offect Veltage due to change in Supply Voltage producing it, keeping other power supply veltage constant. PSRR = AVios AVCC VEE constant. Block diagram of I C. op-Amp. > Stage > > Intermediate -> Stage > Bufferf level chifting Jupert 1 + Stage Now, a days op-amps are available in an integrated Circuit Jorn. Commercial integrated circuit op-amps usually consists of Jour Cascaded plocks. Input Stage , The Input Stage requires high Input impedance to aucid loading on the sources it requires two input terminals, it also requires low output impedance. All such requirements fare achieved by using the dual input, balanced output differential amplipier as the input stayl This stage provides most of the heltage gain of the amplifier.

Date and man Jacque Page 2) Intermediate stage: - The output of the input and intermediate stage drives the next stage which amplifier with Stage. This is another differentia ended output dual input, unbalanced j. e. Single-The overall gain requirement of the opamp high the input stage alone cannot such a high gain. The main function of the intermediate stage is to perouide additional the Veltage gain required. Level Shifting Stage :- All the stages directly coupled to each other As the op-amp amplifie d. c. signals also, the coupling capacitors are not used to cascade. the stages. Hence the d'c- quiescent Ueltage level of perivious Stage gets applied as the input to the next stage. thence stage by stage d. c. lend increases well abour ground petential. Such a high d.c. Uplage level may drive the transites into Saturation. This further may cause distortion in the output due to clipping . This limit the maximum de output Uplage Suring without any distortion level Shifter stage brings H d.c. level down to ground potential, u no signal is applied at the input ter Then signal is quien to last stage which output stage.

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Date 1 Output stage :- The basic requirements of an output 4) Stage are low output Impedance, large are output uchtage Suring & high current sourcing of senking Capability. The push-pull complementary amply fie meets all there requirements of hence used at an output Stage. Op- amp IC 741 pin diagram offsetnull No connection Inuertint Input V+ (+Vce) Non Involvy input output V (-V EZ) offset Null. S Virtual Ground Virtual Ground This means the differential input Veltage Vd between the non inverting 4 inverting input terminal is esentially zero. Ideally SRi = 20  $|Ad = \infty$ Ad = Vo Vd = Vo ( putting Ad = 0) Vd = Vo = 0, V1 = V2 = 0  $V_1 = V_2$ 

Page. Differential amplifier circuit (DC analysis Icher tvee RC RC 2 are matured 0 4 Q Voto -0 Q2 must be exactly 7 qual, into VBt resistances JE hin. equal Rin ZRE Ven N they VEE 2 analysis (Vin = 0 By in loop D use get KVL IBRin -- VBE - 2 IERE + VEE = 0 Ic ~ E Sine 1 VBE Reis ERF VEE -VBE 3 Reis\_f 2RE JEE-VBE Since B 2RF applying KVL at o side we get. ICE - VC-VE

Date Page\_ 1C= VCC - TCRC, -- 6 f-egn & in egn 5 puttin we get CE = VCC -ICRC-VE -7b-Amp Applications Inverting ampli 1 RI R No-4 Ve A=V B=O(Virtual gre die 9d  $R_1 = \infty$ . opamp ue ge Vo RJ Vs Vo RI Vc Vo 0 VS R

Date Page Non inverting amplifier 2 RI TB 744  $\mathcal{V}_{o}$ Vc KCL at node B ue qu VB= Vo-V VB-0 RI VS-0 RI R V 110 R R VS R-RI Ry Vo VS RI J+R Vo VS 3 Teltage of forme Vo ·Vo=

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Date Page. 4) Summin Amp lifie RA R LI Í 12 R2 R3 13 Vo Applying  $\frac{ue get}{1+12+13}$ 0-Vo Rj  $V_1 + V_2$ + V3 K2 R3 Yo = R2 Ŕ R 5) Integrator V Vo 大 KUL we get yin V,-iR $i = \frac{V_{i}}{R} - C$   $\frac{V_{i}}{Q_{i}} = \frac{V_{i}}{V_{i}} - \frac{V_{i}}{Q_{i}} = 0$ -(1)A 0-1

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Page Vo= - Luidt 2 N 4, n (1 <u>Vi</u> dt RCJ udt 1/0 lications of leachical integrator ifferential equations <u>9n voluing</u> <u>9n valog t</u> Various signa 9n Convert haping circuits ramp generator 9n Differentiator 10 JMATOS V Vo KVLme ge applying differential F.t. dt we get オラ

Date / / Page\_ applying KVL we get o-iR = VO - (3) putting egn (2) in egn (2) meget :- $V_0 = -RC dV_i$ applications of Creatical differentiators ) In the mane shaping circuits to detect high frequery Components in the input Signal. 2) As a vate of change detector in For demodulators Input offset Voltage: - Whenever both the input terminal of the op-amp are grounded, Ideally, the output helper should be zero. However, in this Condition, the practical of any shows a small non zero output Veltage. To make this output voltage zero, a small Veltage in millinets is required to be applied to one of the input terminals. Such a voltage makes the output exactly zoro. This dc usltage, which makes the output heltage zero, when the other terminal is grounded is Called input offset Veltage denoted as Vios. Smalls = Doutput = = Vios =

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2 A 1 B Page. Input bias Current Por ideal op-aup, no current flours into the input terminale so input bias current can be defined as the current flowing into each the two input torminals when they are blased tort Same Veltage level i. e. whom the op-amp is baland The two bias currents are never same here the manufactures specify the averge input bies Current its, while is found by adding the magnitudes of Ib, & Ib2 and diverding the Secondary?  $\overline{J}_{b} = [\overline{J}_{b_{1}}] + [\overline{J}_{b_{2}}]$ + op-amb. Input offset Current !-If we supply equal dic currents to the two inputs, output veltage of op-amp must be zero. But practically, there exists some Veltage at the output. To make it zero, the two input currents are made to differ by Small amount. This difference is nothing but the input offset current.  $\overline{Jios} = | \overline{Jb}, -\overline{Jb_2}$ 

Dato / / Paga Output offset hollage Adeally when both the inputs of op-amp are at zero petential, output must be zero. But both input offset heltage of bias current contribute to produce output heltage with zero inputs. The Heltage existing at the output when inputs or Zero is called output offset Voltage 1 denoted as Voos.