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Fundamentals of Microprocessor (EC-403)

8086(Machine Language Instruction Formats)

•A machine language instruction format has one or more number of fields associated with it.

•The first field is called as operation code field or op-code field, which indicates the type of operation to be performed by the CPU

•The instruction format also contains other fields known as operand fields

•The CPU executes the instruction using the information which reside in these fields

•There are six general formats of instructions in 8086 instruction set.

•The length of an instruction may vary from 1 byte to 6 bytes. The instruction formats are described as follows

1 One Byte Instruction:

•This format is only one byte long and may have the implied data or register operands.

•The least significant 3-bits of the opcode are used for specifying the register operand, if any.

•Otherwise, all the 8 bits form an opcode and the operands are implied

2 Register to Register:

•This format is 2 bytes long

•The first byte of the code specifies the operation code and width of the operand specified by 'w' bit.

•The second byte of the code shows the register operands and R/M field, as shown

below.

D7 D1	D0
OPCODE	W

D7 D6	D5 D4 D3	D2 D1 D0
11	REG	R/M

•The register represented by the REG field is one of the operands.

•The R/M field specifies another register or memory location i.e. the other operand.

3 Register to/from memory with no displacement:

•This format is also 2 bytes long and similar to the Register to Register format except for the MOD field as shown.

D7 D1	D0
OPCODE	W

D7 D6	D5 D4 D3	D2 D1 D0
MOD	REG	R/M

•The MOD field shows the mode of addressing. The MOD, R/M, REG and the 'W' fields are decided in Table 2.2.

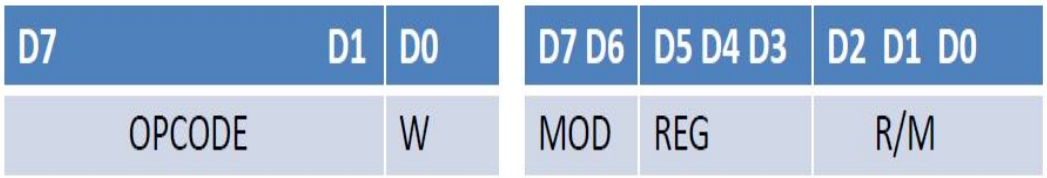
Table 2.2 *Addressing Modes and the Corresponding MOD, REG and R/M Fields*

Operands	*Memory Operands*			*Register Operands*	
	No Displacement	*Displacement 8-bit*	*Displacement 16-bit*		
MOD / *R/M*	*00*	*01*	*10*	*11*	
				W = 0	*W = 1*
000	(BX) + (SI)	(BX) + (SI) + D8	(BX) + (SI) + D16	AL	AX
001	(BX) + (DI)	(BX) + (DI) + D8	(BX) + (DI) + D16	CL	CX
010	(BP) + (SI)	(BP) + (SI) + D8	(BP) + (SI) + D16	DL	DX
011	(BP) + (DI)	(BP) + (DI) + D8	(BP) + (DI) + D16	BL	BX
100	(SI)	(SI) + D8	(SI) + D16	AH	SP
101	(DI)	(DI) + D8	(DI) + D16	CH	BP
110	D16	(BP) + D8	(BP) + D16	DH	SI
111	(BX)	(BX) + D8	(BX) + D16	BH	DI

Note: 1. D8 and D16 represent 8 and 16 bit displacements respectively.
2. The default segment for the addressing modes using BP and SP is SS. For all other addressing modes the default segments are DS or ES.

4 Register to/from Memory with Displacement:

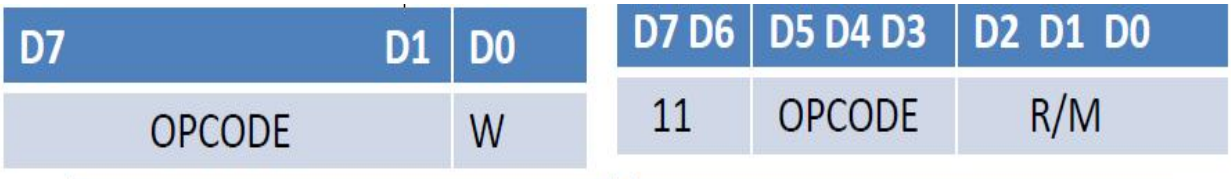
•This type of instruction format contains 1 or 2 additional bytes for displacement along with 2 byte format of the register to/from memory without displacement. The format is as shown below.

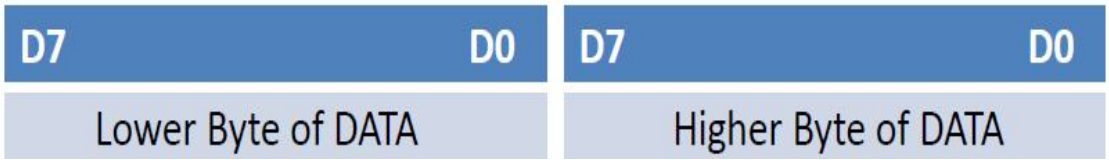


5 Immediate Operand to Register:

•In this format, the first byte as well as the 3-bits from the second byte which are used for REG field in case of register to register format are used for opcode.

•It also contains one or two bytes of immediate data. The complete instruction format is as shown below.





6 Immediate Operand to Memory with 16-bit displacement:

•This type of instruction format requires 5 or 6 bytes for coding.

•The first 2 bytes contain the information regarding OPCODE, MOD and R/M fields. The remaining 4 bytes contain 2 bytes of displacement and 2 bytes of data as shown.