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FET AND MOSFET

Field effect Transistor (FET)

→ The operation of the device depends on electric field intensity produced in the channel.
→ Voltage controlled device
→ High I/P resistance device (≥ 1 M Ω)
→ Power dissipation is very Small.
→ Unipolar device
→ Majority Carriers device.
→ No minority Carriers.
→ Less noisy device than BJT, due to absence of minority Carriers.
→ No leakage Current & therefore temperature effect on the device is very less & therefore excellent thermal stability.
→ fabricated only with Si
→ When compare to BJT, FET is Small in size & easier to fabricated.

Disadvantage :-

→ Smaller gain
→ Smaller gain bandwidth product.

Region of FET

Source :- It is the Source of majority Carrier. i.e. it is the ~~terminal~~ by which majority Carrier will be entering into device
Drain :- It drains of majority Carrier. It is the terminal by which majority Carrier will be leaving the device
Gate :- It is terminal which Control majority

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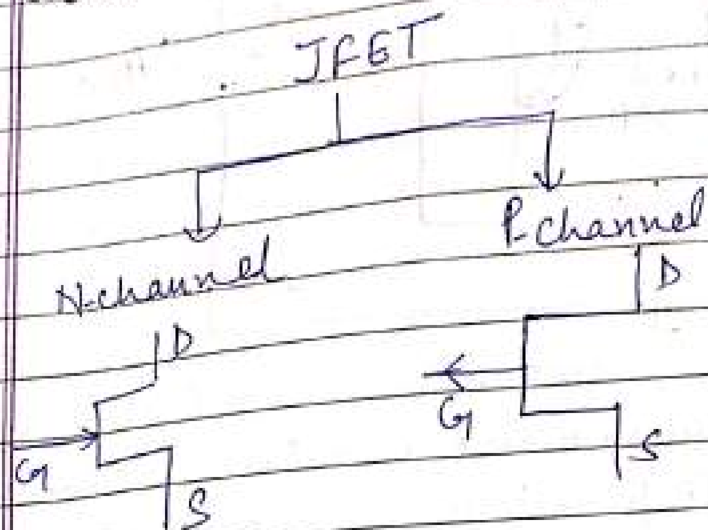
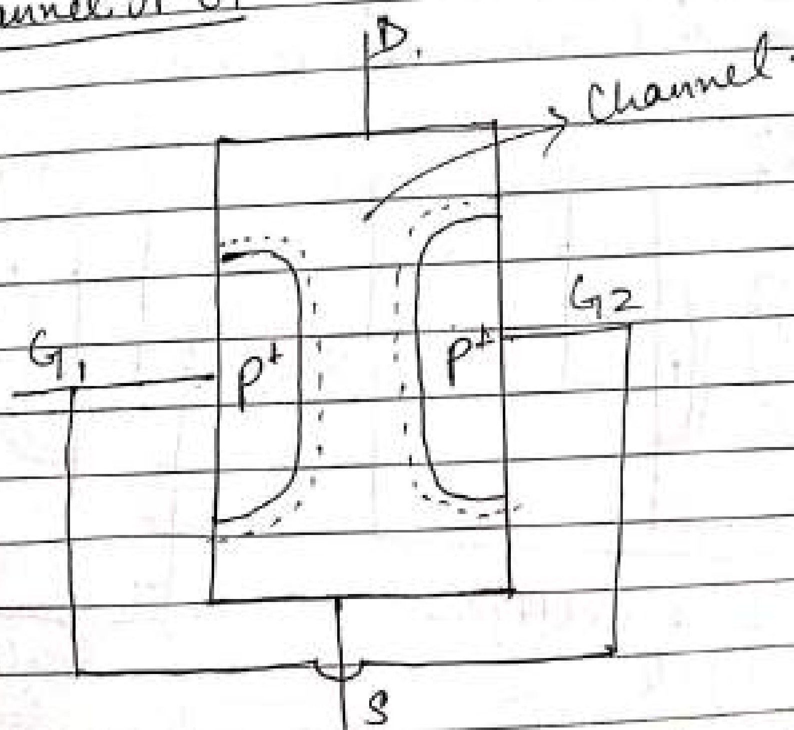
Carriers moving from source to drain.

Channel :- It is the region b/w the two gates.



N-channel JFET



→ When JFET is open circuited, channel cross sectional area is maximum & therefore channel current density is minimum.

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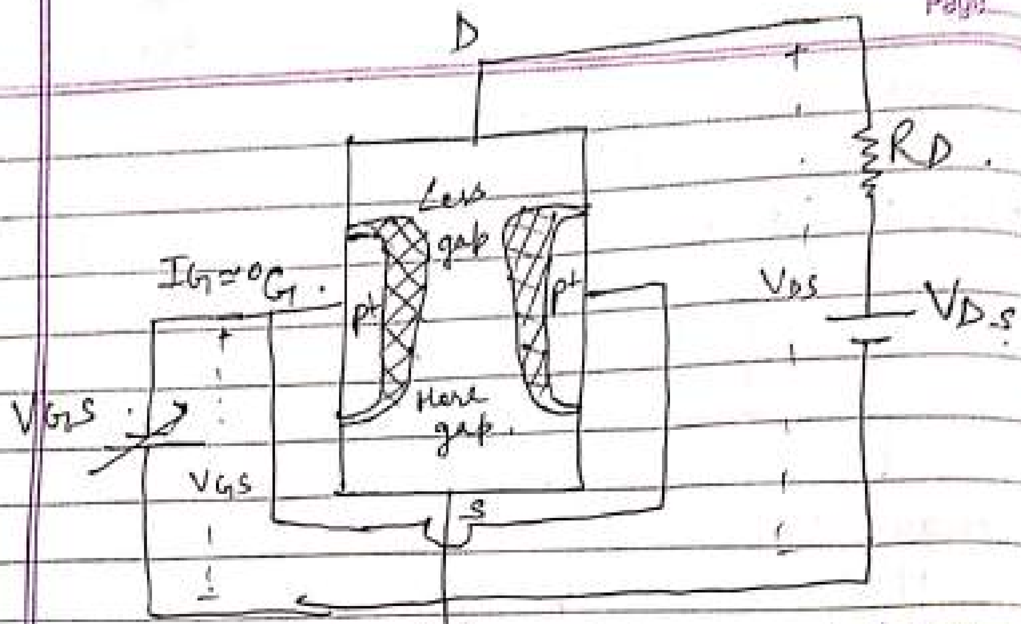
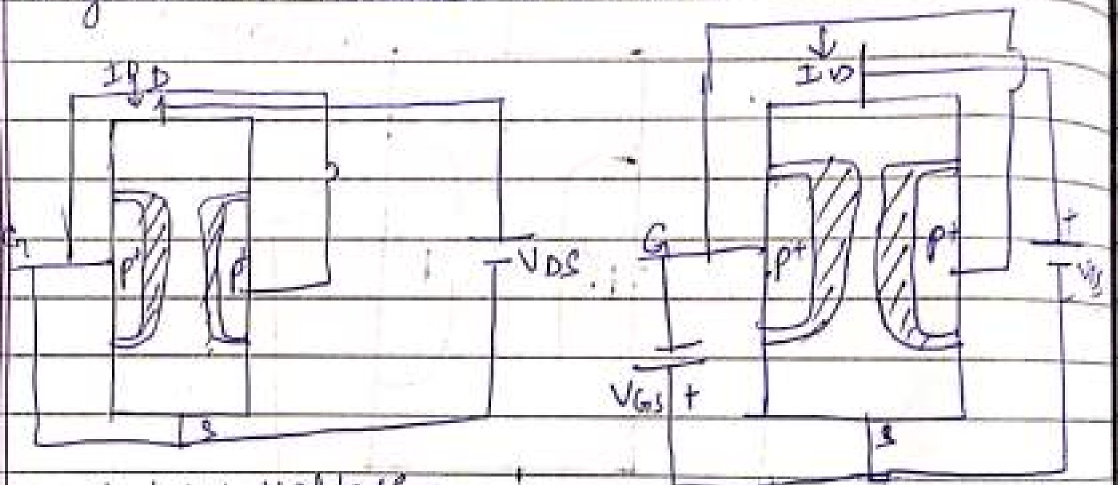
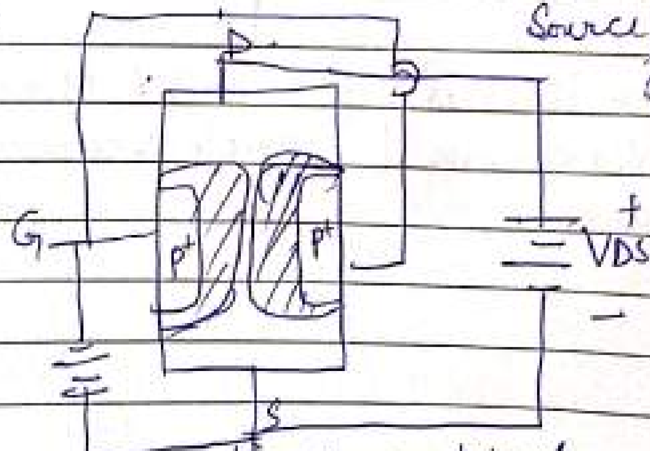


In JFET, the p-n junction between gate & Source is always kept in reverse biased Conditions. Since Current in a reverse biased p-n junction is extremely Small, practically zero, the gate Current in JFET is often neglected & assumed to be zero.



No bias voltage on gate

Small negative gate Source bias. fig (a)



Large negative gate Source bias fig (b)

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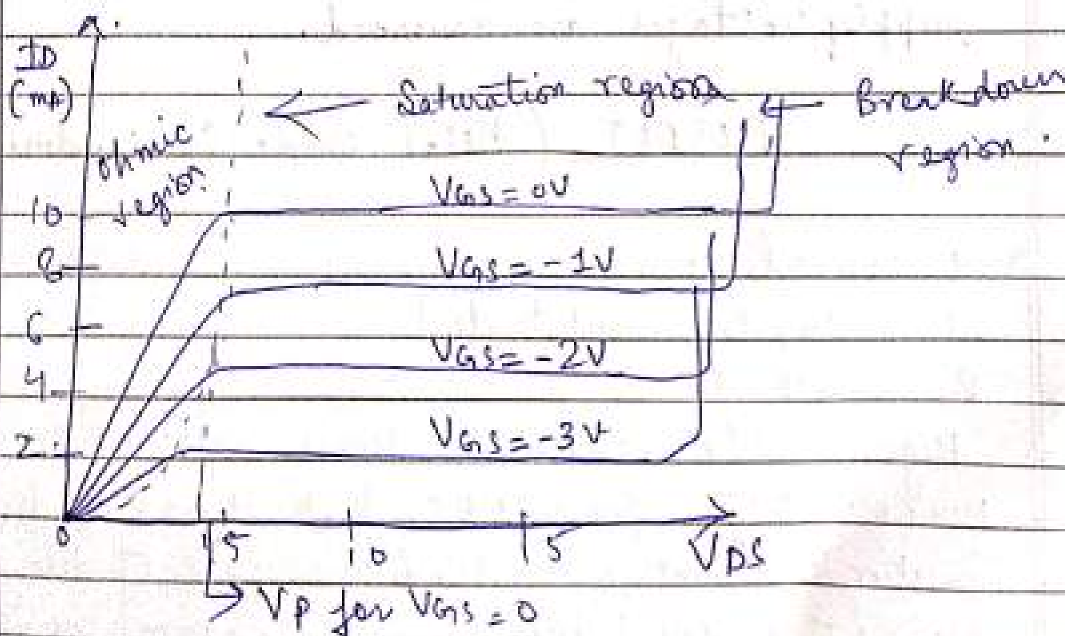
→ when gate to source voltage (V_{GS}) is applied by a dc. supply (V_{GG}) and increased above zero as depicted in fig(a) the reverse bias voltage across the gate-source junction is increased. Because of this depletion regions are widened. This reduces the effective width of the channel & hence controls the flow of drain current through the channel.

→ when gate to source voltage is further increased, a stage is reached at which two depletion regions touch each other as shown in fig (b). This condition is called pinch off.

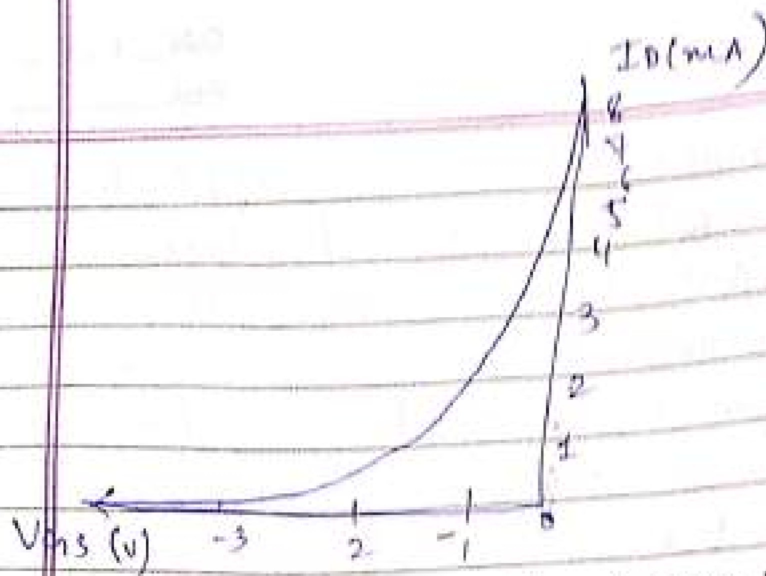
<u>Pinch off voltage (V_P)</u>: It is minimum value of VDS required where ID enters into saturation for given value of VGS.

<u>$V_{GS(off)}$</u> the cut off voltage is the value of V_{GS} at which drain current is zero.

$V_{GS} = |V_P|$



Drain characteristics of n channel JFET



Transfer characteristics of n channel JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The relationship b/w I_D & V_{GS} is non linear this relationship is defined by Shockley's equation.

Note:- The operation of P-channel JFET is exactly similar to N-channel JFET except that the current carriers are holes & polarity of supply voltages are reversed.

MOSFET (Metal oxide Semiconductor FET)

→ 4 channel devices
(S, G, D, Substrate)

→ $R_i = 10^{10}$ to $10^{15}\,\Omega$

→ Highest I/P resistance device is MOSFET

→ MOSFET differs from JFET in that it has no pn junction structure instead the gate of the MOSFET is insulated from the channel by SiO_2 layer.

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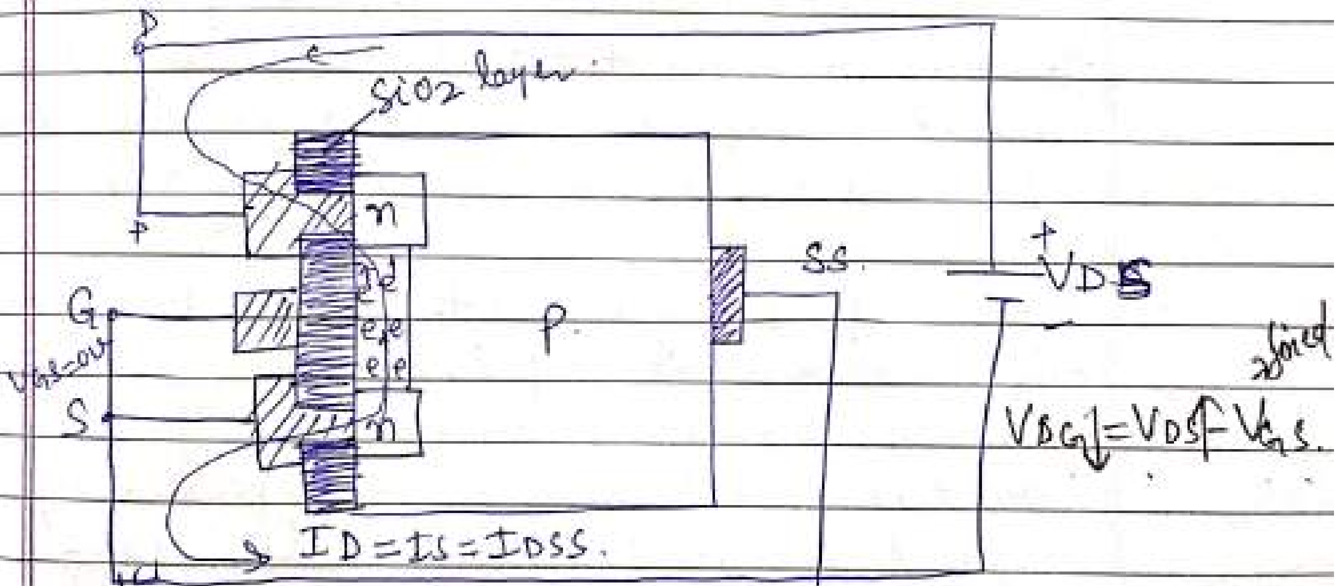
MOSFET

Depletion MOSFET	Enhancement MOSFET
→ there is a pre-existing channel.	→ no pre existing channel
→ Suitable to operate in the depletion mode & enhancement mode.	→ Suitable to operate in the enhance mode only.

→ Input resistance of MOSFET > Input resistance of JFET
→ Power dissipation is less < Power dissipation in JFET.

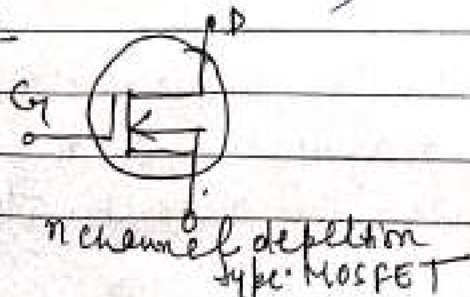
Depletion MOSFET (D-MOSFET)

1) n channel Depletion MOSFET.

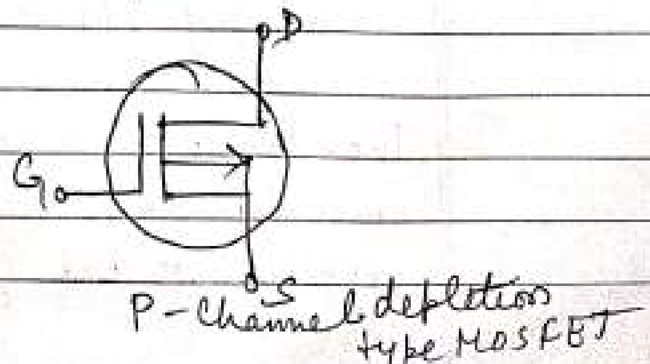


fig(2)a)

Symbol



n channel depletion type MOSFET



P-Channel depletion type MOSFET

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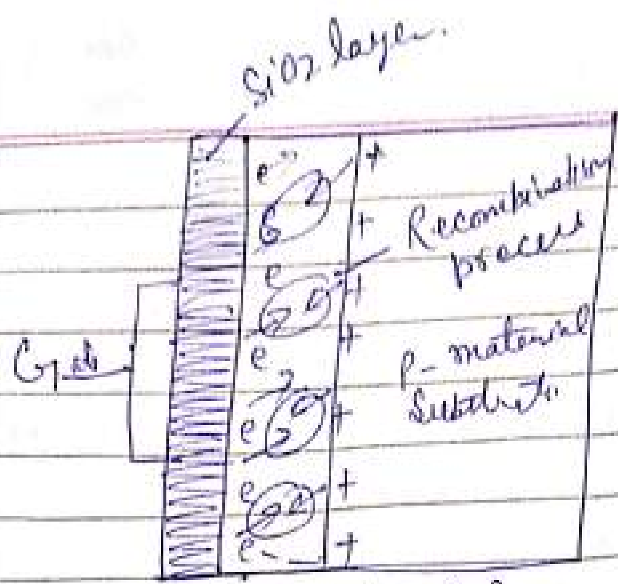

fig 2(b)

(Reduction in free electrons in the n channel due to negative potential at the gate terminal)

→ On the application of drain to source voltage, VDS & keeping gate to source voltage to zero by directly connecting gate terminal to source terminal, free electrons from the n channel are attracted towards positive terminal of drain terminal. This establishes current through the channel to be denoted as IDSS at $V_{GS} = 0V$ as shown in fig 2(a).

→ if we apply negative gate voltage, the negative charges on the gate repel conduction electrons from the channel & attract holes from p type substrate. this initiates recombination of repelled electrons & attracted holes as shown in fig 2(b).

→ The level of recombination between electrons & holes depends on the magnitude of negative voltage applied to the gate. This recombination reduces

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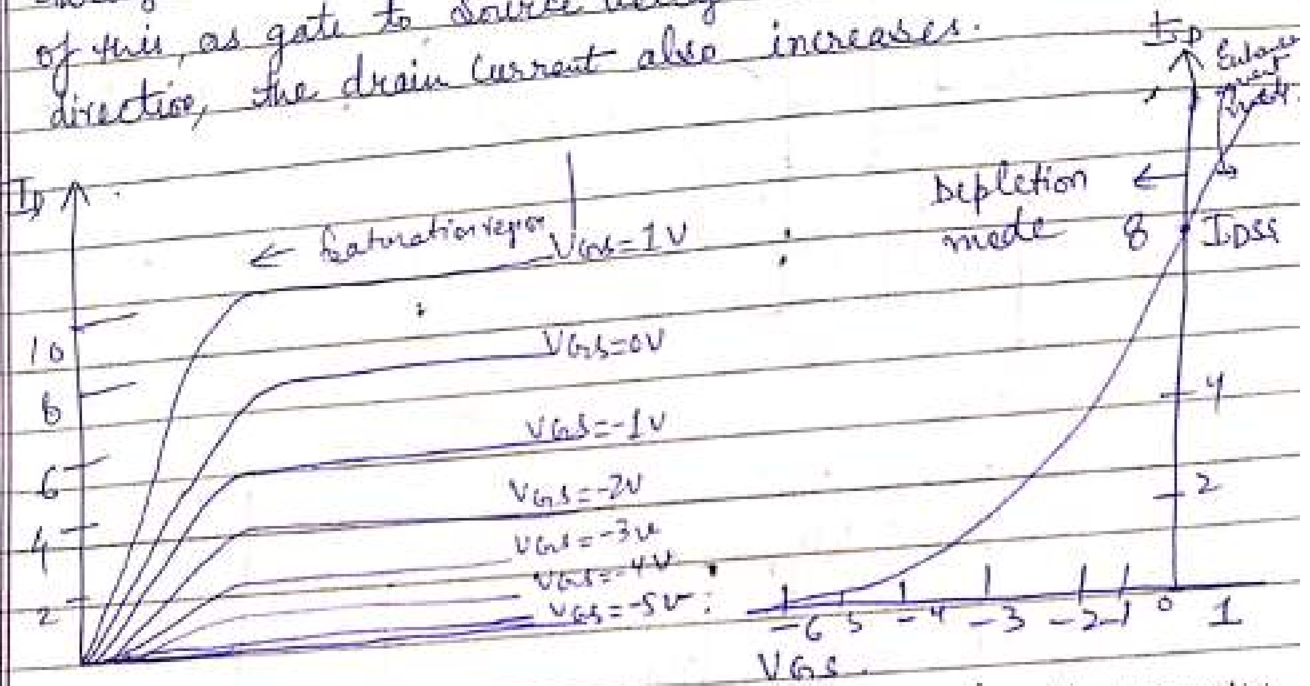
the number of free electrons in the n channel for the conduction reducing the drain current.

For positive value of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current & establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in +ve direction, the drain current also increases.



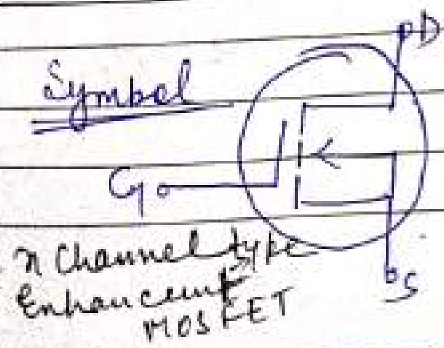
Drain characteristics for an n channel depletion type MOSFET

Transfer characteristics for n channel depletion type MOSFET.

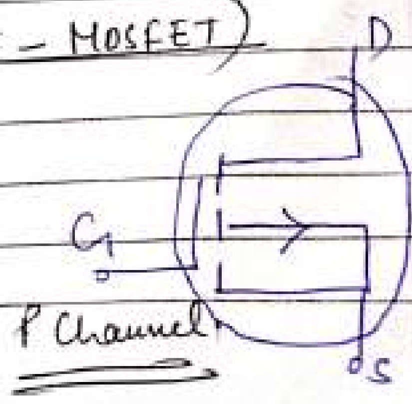
Note:- operation of P-channel Depletion MOSFET is exactly similar to N-channel ~~FET~~ Depletion MOSFET except that of current carriers + polarity of supply voltage.

Enhancement MOSFET (E-MOSFET)

Symbol

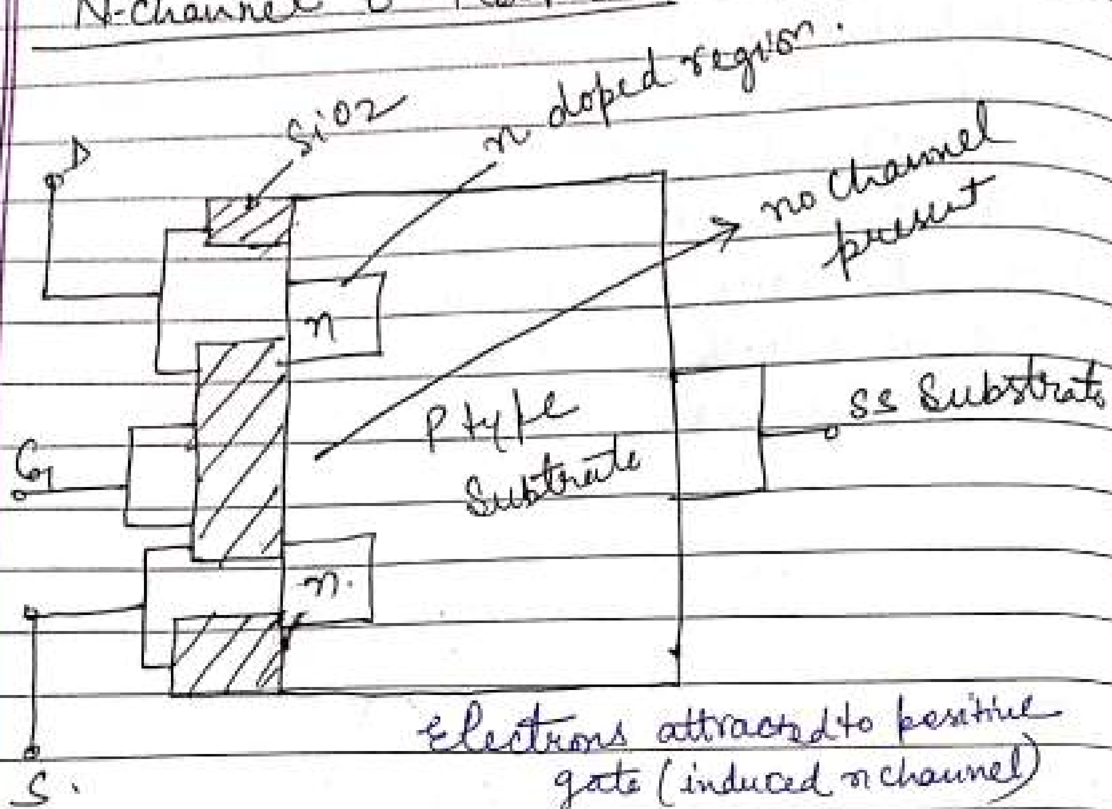


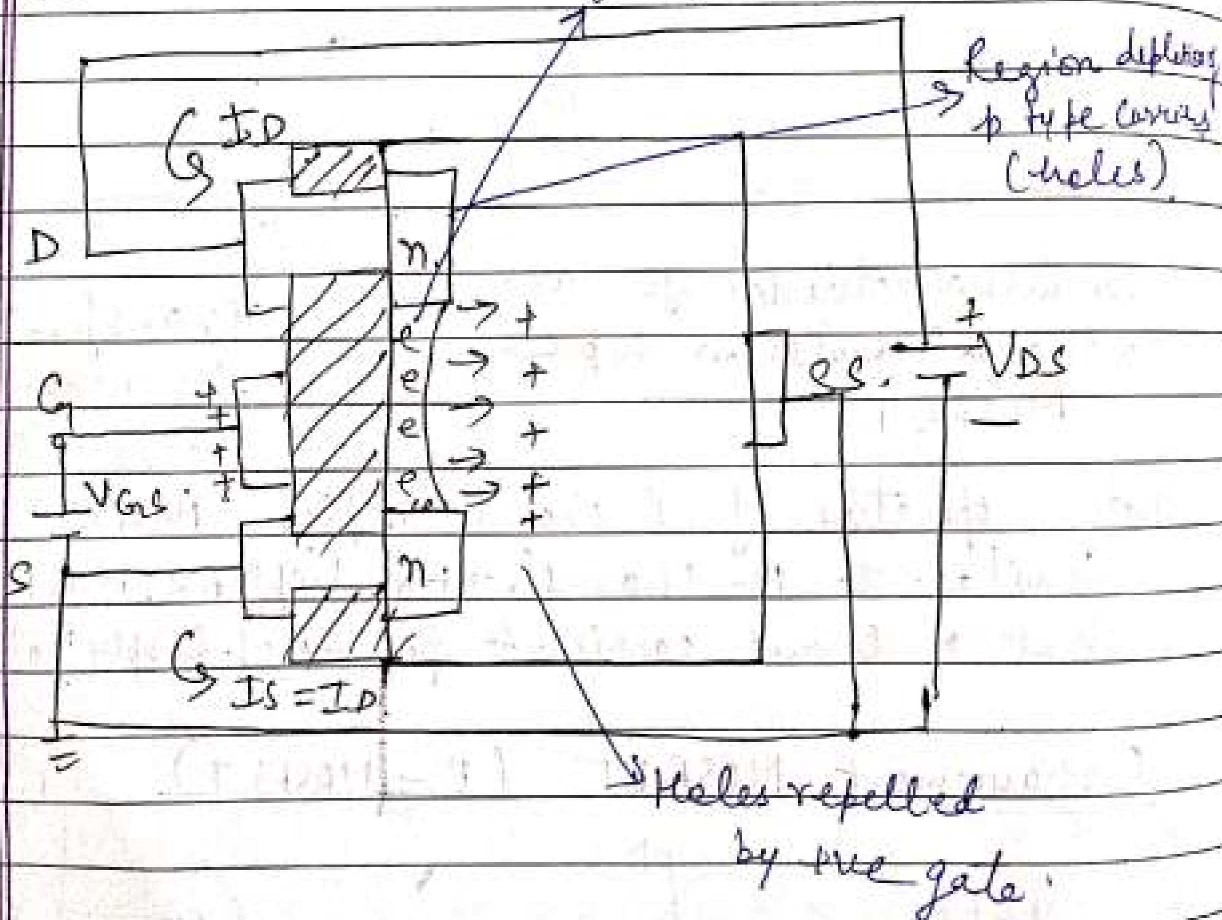
n channel type Enhancement MOSFET



P Channel

N-channel E-MOSFET





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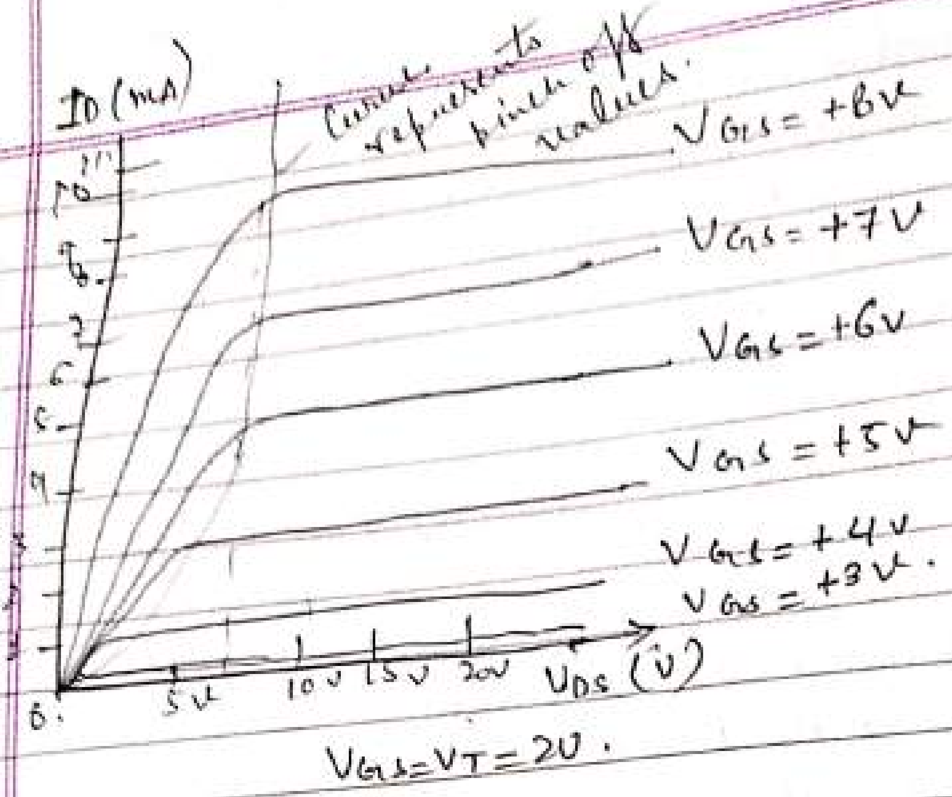
→ On application of drain to source Voltage V_{DS} & keeping gate to source Voltage zero by directly connecting gate terminal to the source terminal, practically zero Current flows quite different from the depletion type MOSFET & JFET.

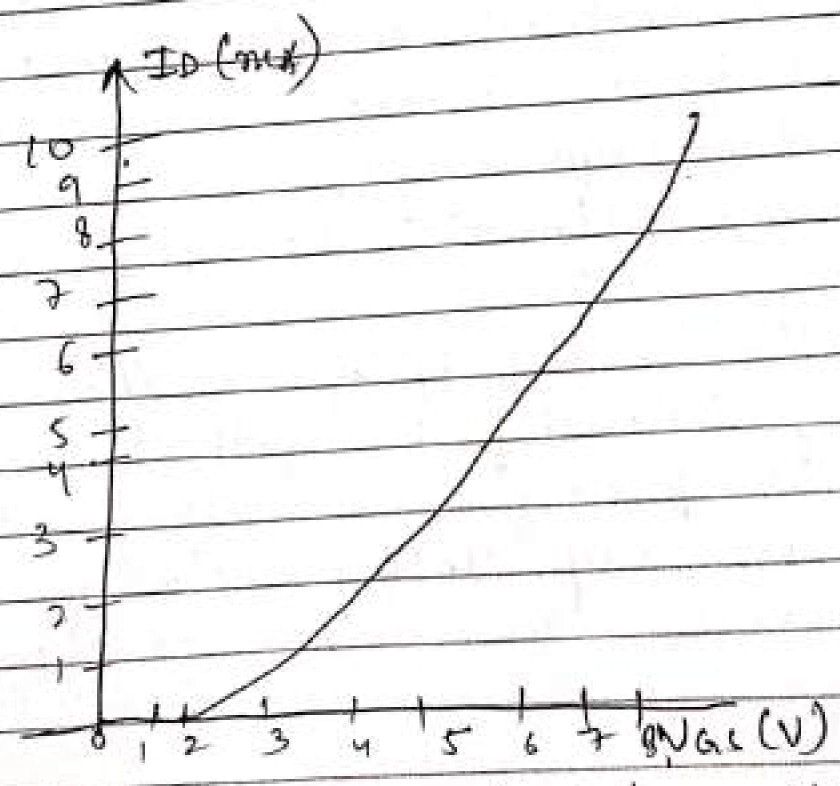
→ If we increase magnitude of V_{GS} in the positive direction the concentration of electrons near SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain & Source. This value of V_{GS} is Called threshold Voltage denoted by V_T.

→ Thus we Can say that in an enhacement type n channel MOSFET, a positive gate Voltage above a threshold value induces a channel and hence the drain Current by creating a thin layer of negative charges in Substrate region adjacent to the SiO_2 layer.

→ The Conductivity of the channel is enhanced by increasing the gate to Source Voltage & thus pulling more electrons into the channel. For any Voltage below the threshold Value, there is no Channel.



Drain characteristics of an n-channel enhancement type MOSFET.



Transfer characteristics for n channel Enhancement type MOSFET.

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