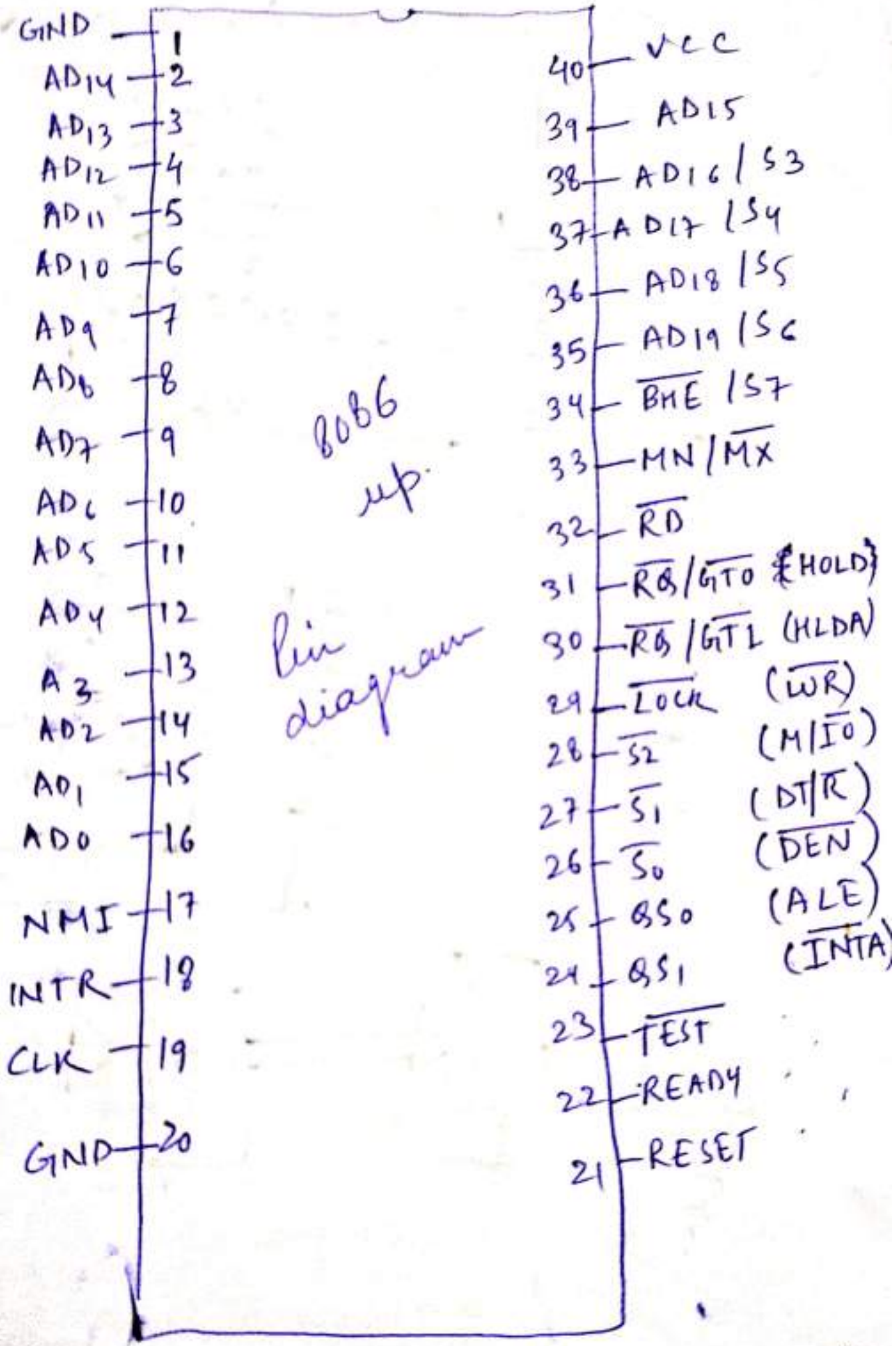

$AD_{15} - AD_0$ → These are the time multiplexed memory I/O address and data lines. address remains on the lines during T_1 state, while data is available on the data bus during T_2, T_3 / T_W & T_4. Here T_1, T_2, T_3, T_4 and T_W are the clock states of a machine cycle.

$A_{19}/S_6 - A_{16}/S_3$ → These are time multiplexed address & status lines ~~during~~ T_1. S_6 is always remains a logic 0.

S_5 → indicate condition of IF flag bits.

S_4, S_3 → show which segment is accessed during current ~~instruction~~ bus cycle.

S_4	S_3	Function
0	0	Extra Segment
0	1	Stack Segment
1	0	code or no segment
1	1	Data Segment.

The address bits are separated from the status bits using latches controlled by the ALE signals.

$\overline{RD}$ → Read Signal (active low pin). when this pin is activated
→ data bus receive data from memory or I/O device for $RD = 0$.
→ high impedance state → during a hold acknowledge

READY → Active High pin.
→ up enter into wait state & remain idle when Ready = 0
→ no affect on the operations of up = Ready = 1.

INTR : interrupt Request.
→ used to request a hardware interrupt.
→ if INTR is held high when IF = 1 ; up enter interrupt acknowledge cycle (INTA become active) after current instruction has complete execution.

~~TEST~~ (BUSY) → tested by WAIT instruction if this pin goes low, then execution will be continued else remains in idle state

NMI → non maskable interrupt.
- Similar to INTR except that no check If flag bit
- if NMI is activated : use interrup vector 2.

RESET → (Active high)
up:reset if RESET held high for a minimum of four clock

CLK (clock) → provide basic timing for processor operation and bus control activity

VCC (power Supply) = +5 V power supply for the operation of the internal circuit.

GND → ground for the internal circuit.

MN / $\overline{MX}$ → the logic level at this pin decides whether the processor is to operate in either minimum (Single processor) or maximum (multiprocessor) mode.

$\overline{BHE}$/S7 : Bus high enable.
→ enable most significant data bus bits (D15-D8) during read or write operation.
→ Status of S7 → always a logic 1.

BHE	A0	Indication
0	0	whole word
0	1	Upper Byte from/to odd address
1	0	Lower Byte from/to Even address

Minimum Mode PINS None.

M/$\overline{IO}$ → Select memory or I/O.

$\overline{INTA}$ (interrupt acknowledge) → response to INTR input pin, normally used to gate interrupt vector no onto data bus.

ALE → This Signals indicates the availability of valid address on Multiplexed lines & is connected to latch enable I/p of latches.

$\overline{DT}/R$ (Data Transmit / Receive) → This output signal indicates the availability of valid address on the. This output is used to decide the direction of data flow through the transreceivers (bidirectional buffer. when processor sends out data this signal is high and when processor is receiving data it is low.

$\overline{DEN}$ → Data Enable :→ This signal indicates the availability of valid data over the address / data lines it is used to enable the transreceivers (bidirectional buffers) to separate the data from the multiplexed address / data signal.

HOLD → when the HOLD line goes high it indicates processor that another master is requesting the bus access.

HLDA (Hold acknowledge) After receiving the HOLD request, the processor issues the acknowledge signal on HLDA pin.

Maximum Mode Unit

MN / $\overline{MX}$ = 0

$\overline{S2}$, $\overline{S1}$, $\overline{S0}$: these lines indicate the type of operation Carried out by the processor

S_2	S_1	S_0	Function.
0	0	0	interrupt acknowledge.
0	0	1	I/O Read
0	1	0	I/O write
0	1	1	Halt.
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	passive.

$\overline{RT}/GT_1$, $\overline{RQ}/\overline{GT0}$ → request / grant) :- request

DMA.

→ bidirectional, request & grant DMA operation.

→ these pin are used by local bus masters, in maximum mode to force the processor to release local bus at the end of processor current cycle

$\overline{LOCK}$ (lock output) :→ this output pin indicates that other system bus masters will be prevented from gaining the system bus while the $\overline{LOCK}$ signal is low.

QS_1, QS_0 → Queue Status.

This lines gives the information about the status of code prefetch queue. these are active high during CLK cycle after which queue operation is performed.

QS_1	QS_0	Indication
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty queue
1	1	Subsequent byte from queue.

8085	8086
1) It is 40 pin IC	→ It is 40 pin IC, high speed HMOS technology
2) Based on NMOS tech	→ Based on HMOS technology
3) Vcc = +5V	→ Vcc = 5V.
4) operating freq = 3MHz	→ operating freq = 5MHz
5) It is 8 bit up.	→ it is 16 bit up.
6) Address pin = 16, data pin = 8	→ Address pin = 20, ~~data pin~~ data pin = 16.
7) Max memory that can interface = 64K Byte	→ Max. memory that can interface = 1MByte.
8) Flag reg. of 8 bit	→ Flag reg 16 bit
9) No. of flags → 5	→ No. of flag = 9.
10) Size of flag register = 8 bit	→ Size of flag register = 16 bit
11) Does not support pipelining.	→ ~~Does not~~ support pipelining.
12) Normal memory Concept is used.	→ Memory Segmentation Concept is used

8086 Interrupts

Date __/__/__
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Interrupt :- the process of interrupting the normal execution of the program to carry out the specific task called interrupt.

Interrupts

- Hardware interrupts
  - Maskable interrupt
    - INTR
  - Nonmaskable Interrupt
    - NMI
    - as soon as NMI occurs the processor has to stop the main program to execute the NMI service routine.
- Software Interrupts
  - 256 types of Software interrupt
    - INT 00 — INT FFH
    - 010H Type 4 pointer overflow
    - 00CH type 3 pointer 1 byte INT instruction.
    - 008H type 2 pointer non maskable
    - 004H type 1 pointer Single step
    - 000H → type 0 pointer Divide error.

Five interrupts are reserved for special purpose.

07FH → type 5 to type 31 are reserved for future use by processor.

type 32 to 255 are free for user.