SYSTOLIC ARCHITECTURE

A network of PEs that rhythmically produces and pass data through the system is called systolic architecture. It is used as a co-processor in combination with a host computer and the behavior is analogous to the flow of blood through heart; thus named SYSTOLIC.

· A systolic architecture has the following characteristics:

- A massive and non-centralized parallelism
- Local communications
- Synchronous evaluation

· Example of systolic network

1. Linear network

2. Bi-dimensional network

3. Hexagonal network

Architecture

A systolic array typically consists of a large monolithic network of primitive computing nodes which can be hardwired or software configured for a specific application. The nodes are usually fixed and identical, while the interconnect is programmable. The more general **wavefront** processors, by contrast, employ sophisticated and individually programmable nodes which may or may not be monolithic, depending on the array size and design parameters. The other distinction is that systolic arrays rely on synchronous data transfers, while wavefront tend to work asynchronously.

Unlike the more common Von Neumann architecture, where program execution follows a script of instructions stored in common memory, addressed and sequenced under the control of the CPU's program counter (PC), the individual nodes within a systolic array are triggered by the arrival of new data and always process the data in exactly the same way. The actual processing within each node may be hard wired or block microcoded, in which case the common node personality can be block programmable.

The systolic array paradigm with data-streams driven by data counters, is the counterpart of the Von Neumann architecture with instruction-stream driven by a

program counter. Because a systolic array usually sends and receives multiple data streams, and multiple data counters are needed to generate these data streams, it supports data parallelism.

A **systolic array** is a network of processors that rhythmically compute and pass data through the system. They derived their name from drawing an analogy to how blood rhythmically flows through a biological heart as the data flows from memory in a rhythmic fashion passing through many elements before it returns to memory. It is also an example of pipelining along with parallel computing. It was introduced in 1970s and was used by Intel to make CMU's iWarp processor in 1990.
In a systolic array there are a large number of identical simple processors or processing elements(PEs) that are arranged in a well organized structure such as linear or two dimensional array. Each processing element is connected with the other PEs and has a limited private storage.

Characteristics:

1. **Parallel Computing –**
   Many processes are carried out simultaneously. As the arrays have a non-centralized structure, parallel computing is implemented.
2. **Pipelinability–**
   It means that the array can achieve high speed. It shows a linear rate pipelinability.
3. **Synchronous evaluation –**
   Computation of data is timed by a global clock and then the data is passed through the network.The global clock synchronizes the array and has fixed length clock cycles.
4. **Repetability–**
   Most of the arrays have the repetition and interconnection of a single type of PE in the entire network.
5. **Spatial Locality –**
   The cells have a local communication interconnection.
6. **Temporal Locality –**
   One unit time delay is at least required for the transmission of signals from one cell to another.
7. **Modularity and regularity –**
   A systolic array consists of processing units that are modular and have homogeneous interconnection and the computer network can be extended indefinitely.

Advantages of Systolic array –

- It employs high degree of parallelism and can sustain a very high throughput.
- These are highly compact, robust and efficient.

- Data and control flow are simple and regular.

Disadvantages of Systolic array –

- They are highly specialized and thus are inflexible regarding the problems they can solve.
- These are difficult to build.
- These are expensive.

Systolic Arrays

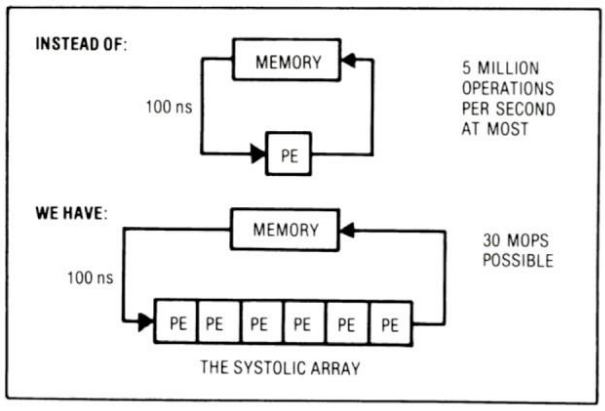

Figure 1. Basic principle of a systolic system.

Memory: heart
PEs: cells

- H. T. Kung, "Why Systolic Architectures?," IEEE Computer 1982.

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